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Multiple resonant controllers strategy to achieve fault ride-through and high performance output voltage in UPS applications

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Abstract: A control strategy to achieve fault ride-through capability and to provide high performance of the output voltage of a single-phase uninterruptible power supply (UPS) inverter is proposed in this study. This strategy consists in controlling the voltage and current waveforms measured at the inverter output filter, with an inner current control loop and an outer voltage control loop, using a plug-in structure based on multiple resonant stages in addition with proportional controllers. In order to achieve stability from no load to short-circuit conditions, the implementation of the multiple resonant controllers includes a compensation of the system phase lag. Moreover, it presents a comparative analysis between two controller structures, the proposed plug-in and the classical proportional + resonant. From this analysis, it can be concluded that the plug-in structure presents improved characteristics of closed-loop output impedance and output voltage dynamic response during fault ride-through events. A controller design methodology to achieve robustness to parametric uncertainties and UPS standard compliance, is detailed. Experimental results from a single-phase 2 kVA inverter prototype are presented to validate the feasibility of the proposal.

1 Introduction

Uninterruptible power supply (UPS) units are mainly designed to feed critical loads such as medical, industrial and computer equipment, in which it becomes necessary to keep an electrical energy of certain quality.

UPS units are composed of power electronic converters, mostly rectifiers and inverters. The latter are mainly used to feed linear and non-linear loads while meeting power quality requirements as well as high robustness and reliability.

Regarding reliability, one of the features that UPS units should have is protection against overload and short circuits. Such protection can be achieved in two ways; the first one is by putting the inverter out of operation once a failure is detected [1], while the second one is to provide the inverter with the ability to maintain a fault current limited to a specific value [2]. The second way allows the UPS inverter to achieve fault ride-through (FRT) capability since the output inverter current is limited until the protection mechanisms clear the fault, re-establishing the normal operation of the remaining loads in a few milliseconds.

Both power quality requirements and FRT can be fulfilled by properly designing the inverter control loops, which is the central issue of this paper.

To achieve the before mentioned features, it is necessary to feedback at the control loops the capacitor voltage and the inductor current of the inverter LC filter. Additionally, it is important to ensure tracking of the reference signals and disturbance rejection. These features can be achieved by including high-gain controllers, which can be linear or non-linear [3, 4].

A possibility to implement linear controllers is the application of the Internal Model Principle (IMP) [5], being the resonant controllers a particular case of this principle [6, 7]. In addition to its transient and steady-state performance characteristics suitable for UPS inverters, these controllers can be designed to achieve high robustness in cases of plant parameters variation [8, 9].

To obtain wide stability margins and fast transient response using resonant controllers, phase compensation must be introduced at each resonant stage [10]. The objective of this compensation is to cancel the phase lag introduced by the plant and the effects of the digital implementation.

To design the resonant controllers that meet the aforementioned goals, different optimisation techniques have been proposed for UPS applications. These proposals lead to remarkable results in terms of robustness to parametric uncertainties, transient and steady-state responses, as well as allow to easily include several performance specifications [8, 9, 11]. The disadvantage of these methods compared to classical control tools, such as frequency response and root locus plots [12–15], is the greatest mathematical complexity to formulate the optimisation problem.

The authors in [16] have presented a design methodology for a control strategy that uses a proportional gain in the inner current control loop and resonant controllers in the outer voltage control loop. In this work, it is shown that using frequency response analysis; the required phase compensation can be established directly from the phase characteristic of the system.

Using a similar control strategy, in [17] different current-limiting schemes to improve the FRT capability of inverters used in microgrids are analysed. Based on the analysis, the authors proposed a current limiting strategy that ensures high power quality with smooth transitions from normal to fault mode and vice versa.

In order to introduce the current limiter in the aforementioned proposal, a large proportional gain is used, what can cause stability problems in cases of digital implementation [18].

In [19–23] it is proposed to include proportional + resonant (PR) controllers in both, the inner and the outer control loops, which allows the disturbance in the output voltage to be rejected and tracking of the inductor current reference. The selective high gain of the resonant controllers in the inner current control loop makes this strategy suitable to introduce current limiters when microcontrollers, or digital signal controllers (DSCs), are used to implement the control strategy.

Particularly in [21], the performance of different current-limiting strategies during FRT events are evaluated, with the aim to establish which scheme leads to the correct operation of the inverter when a fault occurs and then it clears.

When resonant controllers are used in control strategies that provide the inverter with FRT capability, their phase compensation should guarantee system stability in a wide load range, from no-load to short-circuit conditions. One of the contributions of this paper provides a phase compensation that achieves the features mentioned above.

The saturators introduced by traditional current limiting strategies, distorts the output voltage when the output current exceeds the imposed limits. To avoid this distortion in cases of feeding the rated non-linear load, the saturator limits should be set over the peak value of the current drained by this load.

The described situation requires to oversize the UPS output power stage since due to the relationship between the peak values of the rated non-linear load and the rated linear load, the inverter must have the capacity to supply up to 200% of the rated load.

To avoid oversizing the inverter, the second contribution of this paper is a current limiting strategy that limits the control action of the resonant controller implemented at the fundamental frequency. To achieve this feature it is proposed to use proportional gains in a plug-in structure with the resonant stages, instead of the conventional PR. This plug-in structure additionally allows two features to be improved: (i) avoids the use of resonant controllers around the resonant frequency of the *LC* filter and (ii) achieves no overshoot of the output voltage during FRT events.

The third contribution of this paper consists of a design methodology for each controller, which takes into account: (i) the specifications of transient and steady-state responses of the output voltage given by Standards IEC 62040-3 [24], IEC 61000-2-2 [25] and IEEE 519 [26], related to the power quality supplied by the UPS; (ii) the dynamic response of the current control loop; and (iii) robustness to parametric uncertainties.

The remaining part of the paper is organised as follows: Section 2 presents the discrete-time model and the proposed control with current limiting strategies; Section 3 performs an analysis of the proposed control strategy in order to establish the requirements for the phase compensation in each control loop, as well as a comparative analysis between the plug-in and PR control strategies; Section 4 develops a detailed design methodology for each control loop and determines the limiter value for the overload condition; Section 5 presents the experimental results that validate the proposal; finally, conclusions are drawn in Section 6.

2 Description and modelling of the proposed system

Fig. 1*a* shows a graphical representation of the UPS output power stage (inverter, output filter and load) and the controller. In this figure, it can be observed the current and voltage feedbacks of the inverter output filter, which are processed by the controller to generate the command signals for the power semiconductors. The UPS load consists of a linear part, which is known, i_{ok}, and an unknown part, which may be linear or non-linear and is modelled as a disturbance by the current source, i_o.

Fig. 1*b* shows a block diagram, which includes the UPS output power stage and the proposed control strategy.

Taking into account that the switching frequency of the semiconductor switches is significantly higher than the resonance frequency of the *LC* filter, the inverter synthesised voltage v_{ab} is considered as an ideal voltage source. Then, in Fig. 1*b*, the semiconductor bridge is represented by a single gain equal to the DC bus voltage, $V_{\rm dc}$ [27, 28].

As it can be seen in Fig. 1*b*, the controller is composed of two feedback loops: the inner current loop and the outer voltage loop. The controllers based on the IMP, $G_{ci}(z)$ and $G_{cv}(z)$, and the proportional controllers, K_{pi} and K_{pv}, are included in each control loop. This control strategy is based on the structure referred to as '*plug-in*' [29, 30] in the literature.

The K_{pi} control action produces active damping of the dynamics of the inverter output filter, which improves the relative stability and robustness of the system to parametric uncertainties [16].

In the current control loop the controller based on the IMP, $G_{ci}(z)$, is composed of a bank of resonant stages, whose main objective is to track the reference signal generated by the voltage control loop. This tracking process must be guaranteed for all load conditions, including no-load and short-circuit conditions.

The main goal of the proportional controller K_{pv} is to improve the dynamic response of the voltage control loop, keeping robustness to parametric uncertainties, whereas the IMP based controller $G_{cv}(z)$ contains a bank of resonant stages implemented with the aim of rejecting load disturbances.

In order to keep the current limited in cases of overload and short circuits, a limiter is included in the control structure after the proportional controller K_{pv}. This protection allows the inverter to continuously inject the maximum current while maintaining a sinusoidal waveform in steady-state, during short-circuit events.

As follows, the transfer functions corresponding to the UPS output power stage block shown in Fig. 1*b* are defined

$$G_v(s) = \frac{G_1(s)G_2(s)}{1 + G_1(s)G_2(s) + G_2(s)G_3(s)} \tag{1}$$

$$G_i(s) = \frac{G_1(s) + G_1(s)G_2(s)G_3(s)}{1 + G_1(s)G_2(s) + G_2(s)G_3(s)} \tag{2}$$

$$G_{ii}(s) = \frac{G_1(s)G_2(s)}{1 + G_1(s)G_2(s)} \tag{3}$$

$$Z_o(s) = -\frac{G_2(s)}{1 + G_1(s)G_2(s)} \tag{4}$$

where

$$G_1(s) = \frac{I_L(s)}{V_{ab}(s) - V_o(s)} = \frac{1}{sL + r_L} \tag{5}$$

$$G_2(s) = \frac{V_o(s)}{I_L(s) - I_o(s)} = \frac{1}{sC} \tag{6}$$

$$G_3(s) = \frac{I_{ok}(s)}{V_o(s)} = \frac{1}{Z_{Lk}(s)} \tag{7}$$

In (7), $Z_{Lk}(s) = 0$ for the short-circuit condition and $Z_{Lk}(s) = \infty$ for no-load condition.

Fig. 1*b* also shows the effects of the digital implementation through the ideal sampling switches, the zero-order hold (ZOH) and the delays between the sampling times of the measured signals and the update of the control actions, being $T_{\rm s}$ the sampling period [27].

Discretising $G_v(s)$ and $G_i(s)$ using the ZOH method [31], yields

$$G_v(z) = \frac{(1 - z^{-1})}{T_{\rm s}} Z\left\{\frac{G_v(s)e^{-T_s s}}{s}\right\} \tag{8}$$

$$G_i(z) = \frac{(1 - z^{-1})}{T_{\rm s}} Z\left\{\frac{G_i(s)e^{-T_s s}}{s}\right\} \tag{9}$$

For discretising $Z_o(s)$ and $G_{ii}(s)$, the first-order hold (FOH) method is used [16]

$$Z_o(z) = \frac{(z-1)^2}{T_{\rm s} z} Z\left\{\frac{Z_o(s)}{s^2}\right\} \tag{10}$$

$$G_{ii}(z) = \frac{(z-1)^2}{T_{\rm s} z} Z\left\{\frac{G_{ii}(s)}{s^2}\right\} \tag{11}$$

The transfer function $G_{ci}(z)$ proposed in this work is

$$G_{ci}(z) = \sum_{i=1}^{n} \text{FOH}\left\{K_{ri\_I}\frac{s\cos(\theta_{i\_I}) - \omega_i \sin(\theta_{i\_I})}{s^2 + 2\omega_c s + \omega_i^2}\right\} \tag{12}$$

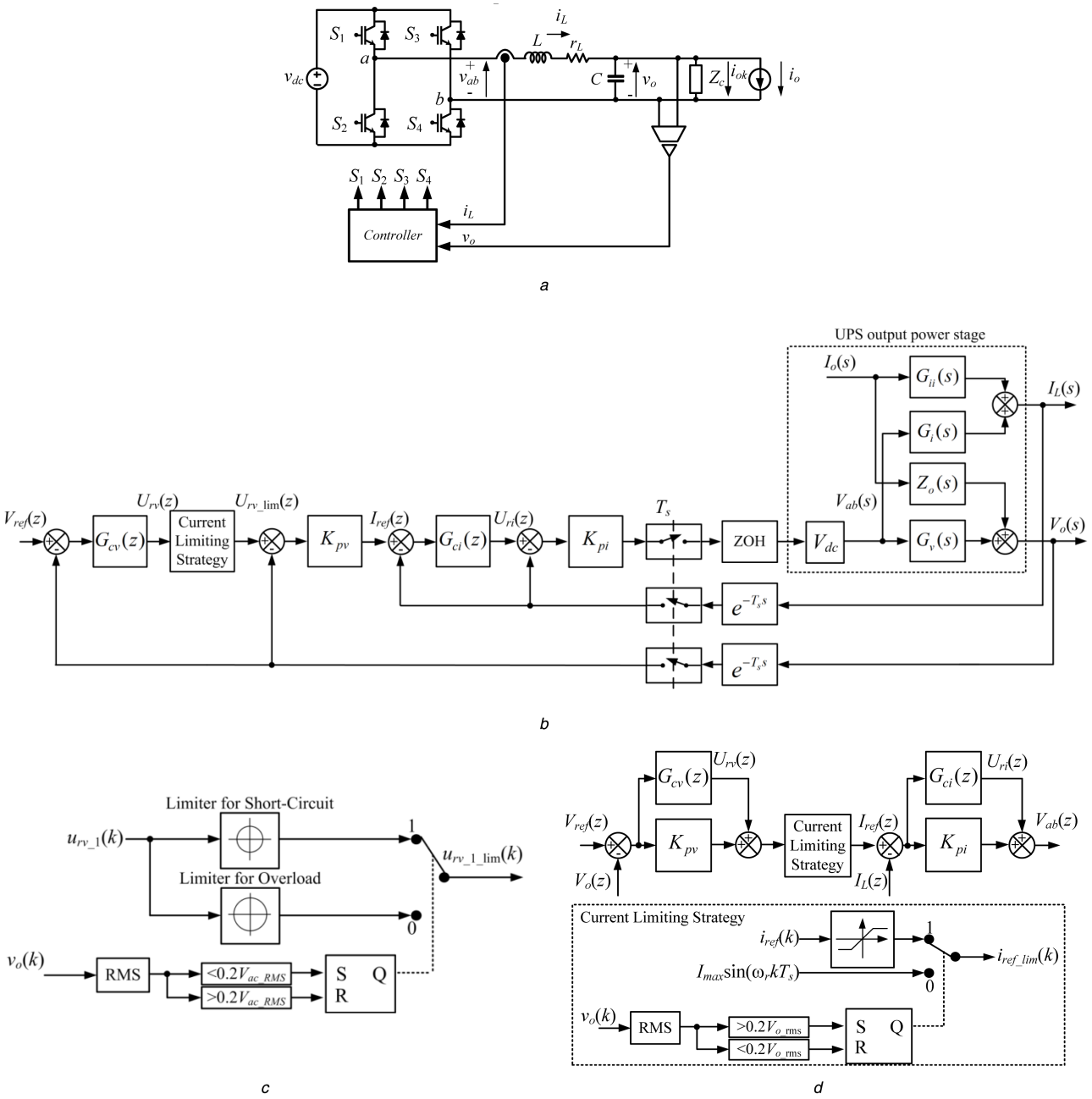

Fig. 1 *Physical and mathematical representation of the system*

(a) Single-phase inverter graphical representation: loads and main variables, ***(b)*** Block diagram of the proposed control strategy and the UPS inverter, ***(c)*** Proposed current limiting strategy to achieve a sinusoidal fault current and avoid inverter oversizing, ***(d)*** Conventional PR control strategy and a proposed current limiting strategy to achieve a sinusoidal short-circuit fault current

This function is composed of the sum of multiple resonant controllers, which form a bank of resonant stages. Discretisation using the FOH method allows a more accurate approximation avoiding the shifting of the resonant frequency and the phase characteristic of the controller [32].

The parameters in (12) are K_{ri_I}, the gain that determines the dynamic response of the current control loop in the ith harmonic component; ω_i, the resonance angular frequency; θ_{i_I}, the angle to compensate the phase lag of the plant [10, 33]; and ω_c, a damping factor normally used to reduce the selectivity at each resonant stage, which facilitate the digital implementation in fixed-point microcontrollers [34], being used in this work $\omega_c = 1$ rad/s.

For the transfer function $G_{cv}(z)$, the following structure is proposed:

$$G_{cv}(z) = \sum_{i=1}^{n} \text{FOH}\left\{K_{ri\_V}\frac{s\cos(\theta_{i\_V}) - \omega_i \sin(\theta_{i\_V})}{s^2 + 2\omega_c s + \omega_i^2}\right\} \qquad (13)$$

where K_{ri_V} and θ_{i_V} are equivalent to K_{ri_I} and θ_{i_I} in (12).

The selection of frequencies ω_i and the design of the remaining parameters are presented in Section 4.

Fig. 1*c* shows the proposed current limiting strategy to achieve a sinusoidal fault current under short-circuit and overload conditions, in addition, to avoid the oversizing of the inverter, since allows the adjustment of the overload limit levels below the peak value of the rated non-linear load.

This strategy uses a set and reset function, activated by the RMS value of the output voltage. When this value is below a threshold level of 0.2 times of the rated RMS output voltage value, $V_{\text{ac\_RMS}}$, short-circuit condition is detected and the limiter value is set to synthesise the short-circuit current under this fault condition, while at the same time resets all the control actions of the resonant stages at each harmonic frequency. When this fault is clear, the output voltage rises until its RMS value is higher than 0.2 times $V_{\text{ac\_RMS}}$, then the limiter value is set back to work for the overload condition.

Table 1 Parameters of the single-phase inverter prototype

output power, S	2 kVA
input voltage, V_{dc}	400 V
output voltage, $V_{ac\text{-}RMS}$	220 V
fundamental frequency, f_r	50 Hz
rated output current, I_{nRMS}	9 A
peak value of short-circuit current, I_{cc}	25 A
base impedance, $Z_{base} = V_{ac\text{-}RMS}/I_{nRMS}$	25.45 Ω
switching frequency, f_{sw}	10 kHz
sampling frequency, f_s	20 kHz
output filter inductance, L	500 μH
inductor resistance L, r_L	0.118 Ω
output filter capacitance, C	60 μF
linear load rated resistance, R_c [a]	24.2 Ω
nonlinear load resistance, R_s [a]	48.4 Ω
nonlinear load smoothing resistance, R_1 [a]	0.97 Ω
nonlinear load capacitance, C_c [a]	3300 μF

[a]According to the Standards IEC 62040-3.

Table 2 Proportional gains of the current and voltage control loops

K_{pi}	7.7×10^{-3}
K_{pv}	0.3

Instead of using instantaneous saturation over the control action, it is proposed to use a distortion-free limiter which operates over the magnitude of the vector composed by the direct and orthogonal component of the corresponding signal [35]. Since the analysed system is a single-phase inverter, to obtain the orthogonal component one of the methods studied in [36] can be implemented. In this paper, all pass filtering tuned to obtain a 90° phase lag at 50 Hz is used.

Section 4 describes how to obtain the limiter values of the distortion-free saturator for both fault conditions.

When conventional PR controller is used in the output voltage control loop, as is the case of shown in Fig. 1*d*, the feed-forward path of the error signal through the proportional gain, does not allow the proposed current limiting strategy to achieve sinusoidal fault current.

To obtain a sinusoidal fault current under short-circuit conditions for the case of conventional PR control strategy, in this paper, it is proposed to switch during this event to a sinusoidal current reference signal, while for the overload condition the saturator actuates directly over the current reference signal. This is shown in Fig. 1*d*, where the same set and reset function of the proposed current limiting strategy for the plug-in control strategy is used. For anti-windup of the resonant controller at the fundamental frequency, tracking integration is used [21].

3 Analysis of the proposed control strategy

This section presents an analysis of the phase compensation requirements for the resonant stages used in the proposed control strategy. In addition, a comparison of transient and steady-state characteristics between the plug-in and PR structures is presented, analysing their closed-loop output impedance and transient recovery of the output voltage during FRT events.

In order to present a qualitative analysis of the system using frequency and time domain responses, the parameters of the inverter and control systems are required. Table 1 includes the parameters of the converter, while the gains and compensation angles of the controllers involved in the control strategy are summarised in Tables 2–4. Section 4 presents the design procedure proposed in this paper to determine these gains.

Table 3 Compensation angles θ_{i_I} and gains K_{ri_I} of the current control loop resonant controllers

θ_{1_I}	−41.1553	K_{r1_I}	700
θ_{3_I}	−33.4597	K_{r3_I}	233.8241
θ_{5_I}	−25.7461	K_{r5_I}	140.8939
θ_{7_I}	−18.0024	K_{r7_I}	101.3007
θ_{9_I}	−10.2166	K_{r9_I}	79.5078
θ_{15_I}	13.4887	K_{r15_I}	49.9702
θ_{21_I}	37.7502	K_{r21_I}	39.0263
θ_{27_I}	62.0897	K_{r27_I}	35.3789

Table 4 Compensation angles θ_{i_V} and gains K_{ri_V} of the voltage control loop resonant controllers

θ_{1_V}	−18.8173	K_{r1_V}	150
θ_{3_V}	−18.7541	K_{r3_V}	23.162
θ_{5_V}	−18.6938	K_{r5_V}	13.7967
θ_{7_V}	−18.6378	K_{r7_V}	8.9361
θ_{9_V}	−12.3036	K_{r9_V}	7.5922
θ_{15_V}	−5.8980	K_{r15_V}	24.0579
θ_{21_V}	0.4624	K_{r21_V}	22.9350
θ_{27_V}	3.3231	K_{r27_V}	98.8961

3.1 Phase compensation for the resonant controllers

The phase lag caused by the system at frequencies ω_i of each resonant stage, has to be compensated with the objective of increasing the relative stability margin and, consequently improving the dynamic response of the closed-loop system.

Considering the inner current control loop, the system phase lag depends on the parameters of the LC filter and the value of the proportional controller K_{pi}. To analyse its phase characteristic, it is proposed to obtain the frequency response of the closed-loop transfer function that relates $i_L(z)$ to $U_{ri}(z)$ (see Fig. 1*b*)

$$G_{pi}(z) = \left.\frac{I_L(z)}{U_{ri}(z)}\right|_{I_o(z)=0} = \frac{K_{pi}G_i(z)}{1 + K_{pi}G_i(z)} \tag{14}$$

To achieve the FRT capability and robustness to parametric uncertainties, the current control loop has to operate stably in the extreme load conditions, from no-load to short circuit. Therefore, $G_{pi}(z)$ should be evaluated for $Z_{Lk}(s) = \infty$ and $Z_{Lk}(s) = 0$ to obtain $G_{pi\_nl}(z)$ and $G_{pi\_sc}(z)$, respectively.

Fig. 2*a* presents the frequency responses of $G_{pi\_nl}(z)$ and $G_{pi\_sc}(z)$, which shows a significant phase difference between no-load to short-circuit conditions in the low-frequency range.

The grey traces of the frequency response shown in Fig. 2*b*, correspond to the open-loop system for the short-circuit condition when $G_{ci}(z)$ contains only one resonant stage tuned at the fundamental frequency, with θ_{1_I} equal to the opposite phase of $G_{pi\_nl}(e^{jTs\omega i})$. It can be observed that the phase margin results in 3.69°.

From this result, it can be concluded that when the compensation angle is established to cancel the phase lag for one of the extreme load conditions (e.g. no-load), it will significantly decrease the relative stability for the opposite extreme load condition (e.g. short circuit).

To observe the effect of a reduced phase margin on the transient response for the particular case of short-circuit condition, a simulation result of the closed-loop transfer function of the inductor current given by

$$G_{i\_cl}(z) = \left.\frac{I_L(z)}{I_{ref}(z)}\right|_{I_o(z)=0} = \frac{G_{ci}(z)G_{pi}(z)}{1 + G_{ci}(z)G_{pi}(z)} \tag{15}$$

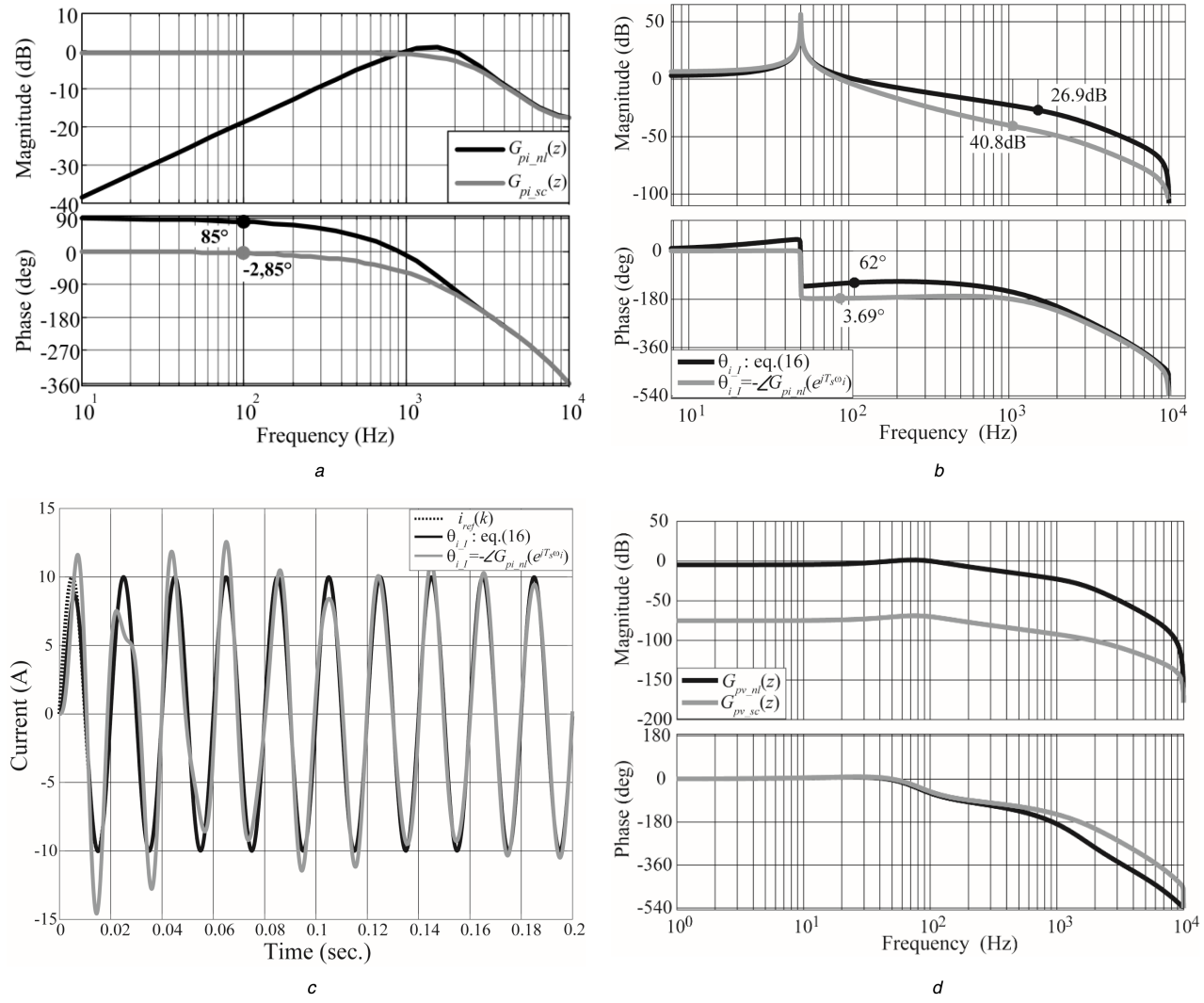

Fig. 2 *Frequency and time responses used for the phase compensation analysis*

(a) Frequency response of the transfer function given by $G_{pi\_nl}(z)$ and $G_{pi\_sc}(z)$ for no-load and short-circuit conditions, respectively, ***(b)*** Frequency response of the open loop system for short-circuit condition, considering $G_{ci}(z)$ with different compensation angles, ***(c)*** Output response of $G_{i\_cl}(z)$ to a sinusoidal input reference signal, being the transfer function evaluated for the short-circuit condition, considering $G_{ci}(z)$ with different compensation angles, ***(d)*** Frequency response of $G_{pv\_nl}(z)$ and $G_{pv\_sc}(z)$, showing similar phase characteristics in the lower frequency ranges

where $\theta_{i\_1}=\angle - G_{pi\_nl}(e^{jTs\omega i})$, is presented in Fig. 2*c*. It can be observed that the inductor current presents a slow and oscillatory response.

Based on the presented analysis, in this paper is proposed to establish the compensation angle as the negative average value of the phase characteristics of $G_{pi}(z)$, obtained for the extreme load conditions

$$\theta_{i\_1} = -\frac{\angle G_{pi\_nl}(e^{jT_s\omega_i}) + \angle G_{pi\_sc}(e^{jT_s\omega_i})}{2} \tag{16}$$

In order to show the improvement of the relative stability margins when the proposed compensation angle is used, the open-loop system frequency response for the short-circuit condition is illustrated with black traces in Fig. 2*b*. It can be observed that the phase margin has been increased up to 62°.

Fig. 2*c* shows a transient response of the current control loop for the short-circuit condition, using the proposed compensation angle. This result indicates that a fast transient response without overshoot can be obtained.

Since the same structure with resonant stages is used in the outer voltage control loop, the analysis of the phase lag to determine the compensation angles is developed in the following paragraphs.

In this case, the control loop with the gain K_{pv} is included in the plug-in structure.

The transfer function that relates $V_o(z)$ to $U_{rv}(z)$, with $I_o(z)=0$ (see Fig. 1*b*) can be expressed as

$$G_{pv}(z) = \left.\frac{V_o(z)}{U_{rv}(z)}\right|_{I_{o(z)}=0} = \frac{G_v(z)G_{ci}(z)K_{pi}K_{pv}}{1 + G_i(z)G_{ci}(z)K_{pi} + G_i(z)K_{pi}(z) + G_v(z)G_{ci}(z)K_{pi}K_{p\backslash}} \tag{17}$$

Fig. 2*d* shows the frequency responses of (17) evaluated in each extreme load conditions. It can be observed that the phase lag at the fundamental frequency presents similar characteristics for both situations.

It can be demonstrated that a reduced value of K_{pv} produces a superior difference between the phase characteristics in the extreme load conditions. For this reason and with the aim of maintaining generality, in this work is proposed to establish the compensation angle as the negative average value of the phase characteristics given by (17), as described below:

$$\theta_{i\_V} = -\frac{\angle G_{pv\_nl}(e^{jT_s\omega_i}) + \angle G_{pv\_sc}(e^{jT_s\omega_i})}{2} \tag{18}$$

where $G_{pv\_nl}(z)$ and $G_{pv\_sc}(z)$ correspond to the transfer function (17) determined for no-load and short-circuit conditions, respectively.

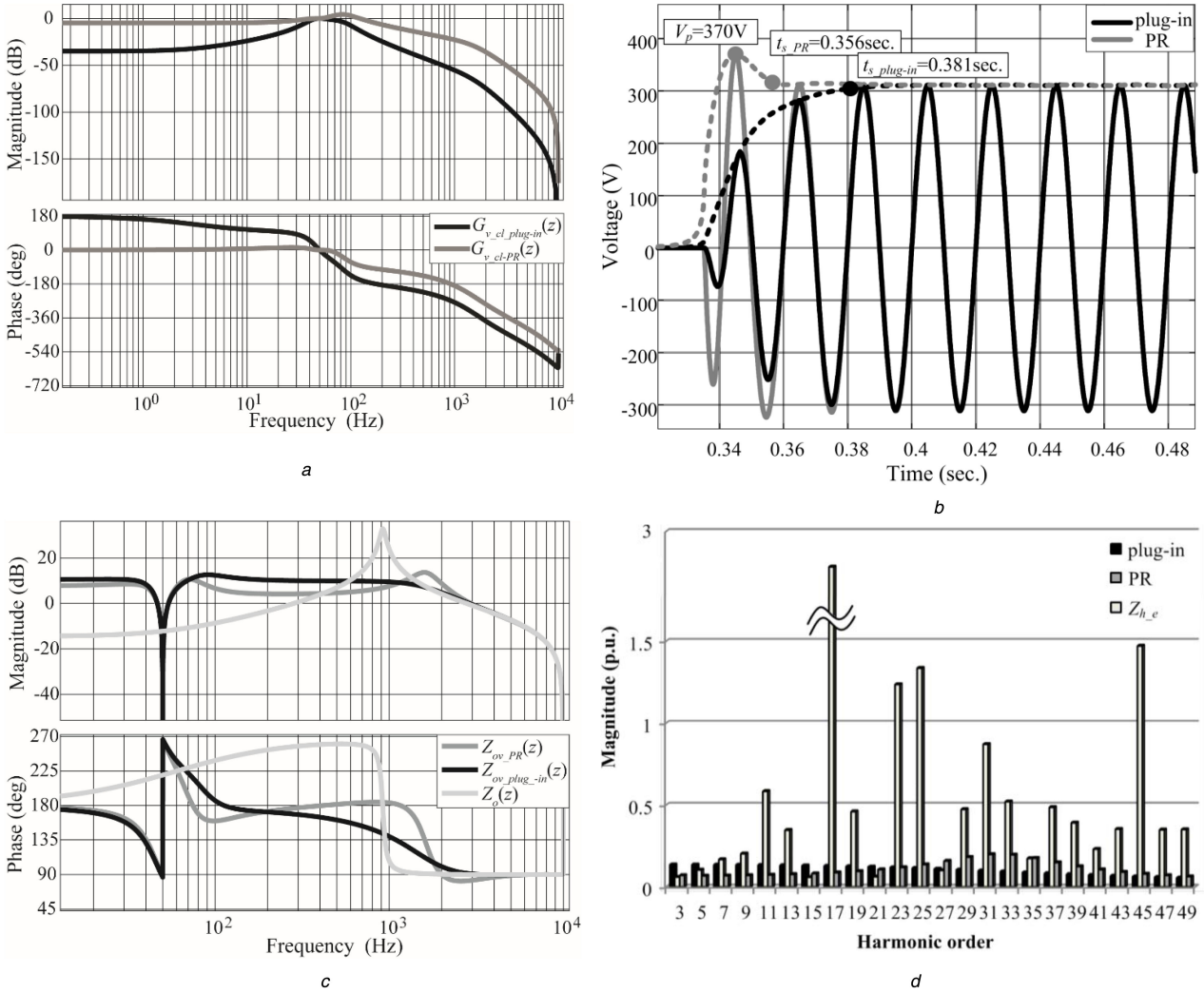

Fig. 3 *Frequency and time responses used in the comparative analysis between the plug-in and PR control strategies*

(a) Frequency responses of the close-loop transfer function that relates the output voltage with the voltage reference signal for the cases of plug-in and PR control strategies, ***(b)*** Transient response of the output voltage during start-up for the two cases: plug-in and PR control strategies, ***(c)*** Frequency responses of the open-loop output impedance $Z_O(z)$, output impedance obtained using the plug-in control strategy in $Z_{ov\_plug\text{-}in}(z)$ and output impedance obtained using the PR control strategy $Z_{ov\_PR}(z)$, ***(d)*** Amplitudes of the inverter output impedance at the harmonic frequencies, $|Z_{ov\_plug\text{-}in}(z)|$, $|Z_{ov\_PR}(z)|$ and harmonic impedance, $Z_{h\text{-}e}$, deduced from the Standards IEC 61000-2-2 and IEC 62040-3, both normalised respect to Z_{base}

As a conclusion, in cases of inverters working with wide load variations, the phase lag at both current and voltage control loops can be compensated at each resonant stage using the negative average value of the phase characteristics of the system, which allows obtaining good results regarding stability and transient response.

3.2 Comparative analysis between plug-in and PR control strategies

In this subsection, frequency and time domain analyses are presented to investigate the differences between the plug-in and PR control strategies when phase-compensated resonant controllers are used.

The closed-loop transfer function that relates the output voltage to its reference signal can be expressed as (see Fig. 1*b*)

$$G_{v\_cl}(z) = \left.\frac{V_o(z)}{V_{\text{ref}}(z)}\right|_{I_o(z)=0} = \frac{G_{cv}(z)G_{pv}(z)}{1 + G_{cv}(z)G_{pv}(z)} \tag{19}$$

Fig. 3*a* shows the frequency response of $G_{v\_cl}(z)$, using both plug-in and PR control strategies. It can be observed that the magnitude of the frequency response using PR control strategy, presents an underdamped response around the frequency ω_i of the resonant controller, being, in this case, $\omega_i = 2\pi 50$ rad/s. On the other hand, when the plug-in control structure is used, it results in a plane magnitude of the frequency response around the same frequency. This fact indicates that no overshoot will be present in the transient response of $G_{v\text{-}cl\_\text{plug-in}}(z)$, as shown in Fig. 3*b*, while for the transient response of $G_{v\text{-}cl\_PR}(z)$, there will be an overshoot as it is shown in the same figure.

The envelopes shown in Fig. 3*b*, with which the overshoot and settling times are established, can be obtained using the discrete-time Hilbert transform [37].

These results show a significant difference of the output voltage using both control strategies, which makes the plug-in structure more suitable to overcome the FRT event, since there will be no overshoot in the output voltage during the transient recovery from short circuit to normal operation.

Another characteristic to be analysed is the closed-loop output impedance of each control strategy, which provides information about the steady-state output voltage distortion in cases of feeding non-linear loads.

The closed-loop output impedance can be obtained from Fig. 1*b*, as the transfer function that relates $V_o(z)$ to $I_o(z)$ with $V_{\text{ref}}(z) = 0$, which results in the expression given by (23) when a plug-in control strategy is used. In the case of PR control structure, the same procedure yields to the expression given by (24).

Fig. 3*c* shows the frequency response of the closed-loop output impedance for each case, as well as the open loop output impedance. In this figure, it can be observed that the magnitude

response for the plug-in control strategy presents a planned response around the resonance frequency of the *LC* filter, while for the PR structure a lobe appears close to the same frequency.

It can be shown that the amplitude of the lobe for the PR structure, depends on the value of the gain K_{pv}, where larger values of K_{pv} increases the magnitude of the lobe. It can be demonstrated that the performance of the steady-state output voltage, concerning the power quality requirements, is affected when the magnitude of the lobe increases.

To analyse this situation, the magnitude of the closed-loop output impedance can be compared with the harmonic impedance defined in [16]. This concept establishes the limits of the impedance magnitude so that the load current flowing through this impedance produces an output voltage with individual harmonic content that meets the standards.

The harmonic impedance can be expressed as

$$|Z_{h-e}| = \frac{|V_{h-\text{limit}}|}{|I_h|} \tag{20}$$

where $|V_{h\text{-limit}}|$ indicates the amplitude limits of the voltage individual harmonic components established by the standards, $|I_h|$ are the individual harmonic components of the current consumed by load and h denotes the harmonic order.

Fig. 3*d* shows the harmonic impedance and the magnitude of the closed-loop output impedance for the two cases, plug-in and PR control strategies, with all these quantities, normalised respect to Z_{base}. The harmonic frequencies where resonant stages should be added correspond to those in which the magnitudes of the closed-loop output impedances are larger than the harmonic impedance.

From this analysis, it can be concluded that the plug-in control strategy requires less resonant stages than the PR structure. In the low-frequency ranges, both strategies share larger magnitude of output impedance in comparison with the harmonic impedance, while only the PR control strategy requires resonant stages in frequencies near the resonance frequency of the *LC* filter.

As a conclusion, the proposed plug-in control strategy presents better characteristics in comparison to the PR structure concerning transient response and steady-state characteristic.

4 Design methodology

This section presents the design procedure for the proposed controller. The methodology is based on the analysis given in [16], which includes specifications for the steady-state and transient responses established by the cited standards, as well as the robustness to parametric uncertainties of the inverter output filter. The main difference between the design methodology of [16] and the one proposed in this paper, resides in the fact that the control strategies are different.

The following subsection introduces design criteria for the resonant stages of the inner current control loop and the proportional gain K_{pv}, which includes the phase compensation analysed in Section 3.1.

4.1 Current control loop design

The procedure for designing the inner current control loop as defined in Fig. 1*b* is described below.

4.1.1 Design of the proportional gain K_{pi}: Gain K_{pi} is determined to relocate the poles of the system in order to achieve the greatest possible damping with this control action, establishing the system robustness to parametric uncertainties of the *LC* filter, according to [16].

4.1.2 Design of the resonant stages $G_{ci}(z)$: As the reference of the inner current control loop comes from the outer voltage control loop, the harmonic components of the reference signal depend on $G_{cv}(z)$. Then, to achieve tracking of $I_{\text{ref}}(z)$, resonant stages must be included in $G_{ci}(z)$ at the same frequencies ω_i as those used in $G_{cv}(z)$.

To select the frequencies of the resonant stages required in $G_{cv}(z)$, it has to be performed the analysis presented in Section 3.2, being the harmonic frequencies those where the magnitudes of the closed-loop output impedance are larger than the harmonic impedance.

For this comparison, the inverter output impedance initially depends on the parameters of the *LC* filter and on the proportional controller in the current control loop. Then using (23) with $G_{ci}(z) = 0$, $G_{cv}(z) = 0$ and $K_{pv} = 0$, $Z_{ov\_plug\text{-}in}(z)$ can be compared with (20) to determine the frequencies where it becomes necessary to design the resonant stages.

The next step is to determine the compensation angles, θ_{i_I}, aiming at compensating for the system phase lag, for which based on the analysis of Section 3.1, it is proposed to use (16) to achieve phase compensation in the inner current control loop from no-load to short-circuit condition.

The following step consists in determining the K_{ri_I} gains of the resonant stages. The speed at which the error converges to zero at each harmonic component is proportional to the gain in the corresponding resonant stage [10]. For this reason, it is firstly proposed to determine the gain of the resonant stage at the fundamental frequency as a function of the desired convergence rate. Then, it is proposed to calculate the gains of the rest of the resonant stages in order to match the convergence error speed at all the harmonic components.

Using Fig. 1*b*, the direct path gain at each harmonic component can be deduced from the closed-loop transfer function (15). Matching the direct path gain at the harmonic frequencies, with the direct path gain at the fundamental frequency, it can be obtained

$$K_{ri\_I}\left|G_{pi}(e^{j\omega_i T_s})\right| = K_{r1\_I}\left|G_{pi}(e^{j2\pi 50 T_s})\right| \tag{21}$$

where

$$K_{ri\_I} = K_{r1\_I}\frac{\left|G_{pi}(e^{j2\pi 50 T_s})\right|}{\left|G_{pi}(e^{j\omega_i T_s})\right|} \tag{22}$$

4.2 Voltage control loop design

Once the current control loop controllers are designed, the design of the voltage control loop controllers is proposed

(see (23))

(see (24))

4.2.1 Design of the proportional gain K_{pv}: The dynamic response of the output voltage to step-load variations depends on both K_{pv} and the gain of the resonant stage at the fundamental frequency. Therefore, it is proposed to determine K_{pv} to guarantee the system robustness to parametric uncertainties, adjusting subsequently the gain K_{r1_V} to obtain the desired dynamic response to linear load steps.

$$Z_{ov\_plug-in}(z) = \frac{(Z_o(z)G_i(z) - G_{ii}(z)G_v(z))K_{pi}(G_{ci}(z)+1) + Z_o(z)}{1 + G_i(z)K_{pi}(G_{ci}(z)+1) + G_{ci}(z)K_{pi}G_v(z)K_{pv}(G_{cv}(z)+1)} \tag{23}$$

$$Z_{ov\_PR}(z) = \frac{(Z_o(z)G_i(z) - G_{ii}(z)G_v(z))K_{pi}(G_{ci}(z)+1) + Z_o(z)}{1 + G_i(z)K_{pi}(G_{ci}(z)+1) + G_v(z)K_{pi}(G_{ci}(z)+1)K_{pv}(G_{cv}(z)+1)} \tag{24}$$

To choose K_{pv}, it is proposed to evaluate the location of the poles in (17) within a range of variation of the LC filter parameters, considering different gains K_{pv}, aiming at guaranteeing the system robustness for the range of parametric variations expected for this application.

Once K_{pv} is obtained, the design of the voltage control loop resonant stages begins.

4.2.2 Design of the resonant stages $G_{cv}(z)$: To determine the parameters of the voltage control loop resonant stages, it is used the methodology proposed by the authors [16]. The compensation angles are determined based on the analysis presented in Section 3.1, whereas K_{r1_V} is determined so that the system can satisfactorily respond to the load-step test required by Standard IEC 62040-3. Finally, gains K_{ri_V} associated with the resonant stages of the harmonic frequencies are determined to reduce the output impedance, in order to meet the UPS power quality requirements.

For the compensation angles, θ_{i_V}, the analysis presented in Section 3.1 establishes (18) to achieve phase compensation in the outer voltage control loop, considering load variations from no-load to short-circuit condition.

In order to determine gain K_{r1_V}, the system performance can be evaluated through numerical simulation considering the transient response of the output voltage during load variation steps specified by the IEC 62040-3. According to the superposition principle, the system response is given by

$$V_o(z) = G_{v\_cl}(z)V_{\text{ref}}(z) + Z_{ov}(z)I_o(z) \tag{25}$$

Therefore, the output voltage transient response can be obtained for different values of K_{r1_V} by evaluating the response of the transfer functions (19) and (23) for the inputs $V_{\text{ref}}(z)$ and $I_o(z)$, respectively.

As for the K_{ri_V} gains corresponding to the fundamental harmonic frequencies, they are determined from the required output impedance. To obtain an expression to calculate these gains, (23) must be solved for K_{ri_V}, obtaining (32), where $G_{ri}^{*}(z)$ is the transfer function for each resonant stage without its corresponding gain.

To calculate K_{ri_V}, the magnitude of $Z_{ov}(z)$ is specified at each harmonic frequency by the experimental determination of a scale factor of $Z_{h\text{-}e}$, denoted as F_{ac},

$$|Z_{ov}(z)| = F_{ac}Z_{h-e} \tag{26}$$

The criterion to determine F_{ac} requires decreasing its value from $F_{ac} = 1$ until the total harmonic voltage distortion (THD_v) reaches a minimum value, after which a decrease in F_{ac} produces an increase of THD_v [16].

4.2.3 Limiter values determination: Two limit values for the distortion-free saturator of the current limiting strategy should be determined, one for the short-circuit condition and the other for the overload condition.

Considering the short-circuit condition, the limit value, U_{sat_sc}, is determined by analysing Fig. 2*b*, where the current reference signal is given by

$$i_{\text{ref}}(k) = [u_{rv\_1}(k) - v_o(k)]K_{pv} \tag{27}$$

where $u_{rv\_1}(k)$ is the control action obtained by $G_{cv}(z)$ considering only the resonant controller at the fundamental frequency. Clearing $u_{rv\_1}(k)$ from (27) is obtained

$$u_{rv\_1}(k) = \frac{i_{\text{ref}}(k)}{K_{pv}} + v_o(k) \tag{28}$$

In the short-circuit condition $v_o(k)$ is practically zero, for which the required value to synthesise the short-circuit current with peak value I_{cc}, is given by

$$U_{sat\_sc} = \frac{I_{\text{cc}}}{K_{pv}} \tag{29}$$

To determine the limit value for the overload condition, U_{sat_ol}, the transfer function that relates $U_{rv}(z)$ with $V_{\text{ref}}(z)$ is obtained from Fig. 2*b* as

$$\frac{U_{rv}(z)}{V_{\text{ref}}(z)} = \frac{G_{cv}(z)\left[1 + K_{pv}G_{pv}(z)\right]}{1 + K_{pv}G_{pv}(z) + K_{pv}G_{pv}(z)G_{cv}(z)} \tag{30}$$

where $G_{pv}(z)$ should be determined with the highest allowed overload current. Evaluating (30) at the fundamental frequency, U_{sat_sc} is given by

$$U_{sat\_sc} = \left|\frac{U_v(e^{j2\pi 50T_s})}{V_{\text{ref}}(e^{j2\pi 50T_s})}\right| V_{\text{p}} \tag{31}$$

where V_{p} is the peak value of the rated output voltage.

5 Experimental results

To validate experimentally the proposed control strategy, a prototype shown in Fig. 4*a*, was implemented with parameters given in Table 1. This experimental setup has the capability to operate as a three-phase four-wire inverter, used as a single-phase DC–AC converter in this work.

The designed controller's parameters with the methodology presented in Section 4 are shown in Tables 2–4. It can be observed that besides the required resonant stages in 3rd, 5th, 15th, 21st and 27th, resonant stages at 7th and 9th harmonic have been added with the objective to improve the THD_v.

The controller was implemented in a DSC TMS320F28335, operating at 150 MHz and using floating-point arithmetic. The total measured computation time of the control algorithm was 18.8 µs (see (32)) . Fig. 4*b* shows a window comparator implemented to obtain a trip-zone signal, which triggers the DSC to operate with cycle-by-cycle tripping, used for current limiting when this variable goes higher and lower than maximum and minimum window limits.

This circuit is required for the case of using conventional PR control strategy, since the current limiting strategy presents a high transient inductor current causing the protections of the semiconductor drivers to trip, taking the UPS out of operation.

5.1 Experimental results of the plug-in control strategy

Figs. 5*a* and *b* show for the case of using plug-in control strategy, the transient responses of the output voltage and of the load current for a variation of 20–100% and 100–20% of the rated load, respectively. These tests correspond to the requirements of the standards IEC 62040-3 [24] for step linear load transients.

The data shown in Fig. 5*c* were obtained as a function of the results shown in Figs. 5*a* and *b*. This figure shows the percentage deviations of the RMS output voltage with respect to its rated value during the load variation tests. In addition, the same figure shows the limits required by Classification 1 of the standard IEC 62040-3. It is possible to observe in both traces that the deviation obtained with the experimental prototype does not exceed 8% of the rated value, which largely satisfies the requirements of the standard.

Fig. 6*a* shows the output voltage and the load current obtained when the inverter operates in a steady-state supplying a non-linear reference load, normalised according to IEC 62040-3.

Fig. 6*b* shows the harmonic content of the inverter output voltage and the individual harmonic content limits required by IEC 61000-2-2, indicating the compliance with UPS power quality requirements. The THD_v was computed and it results in 2.23%,

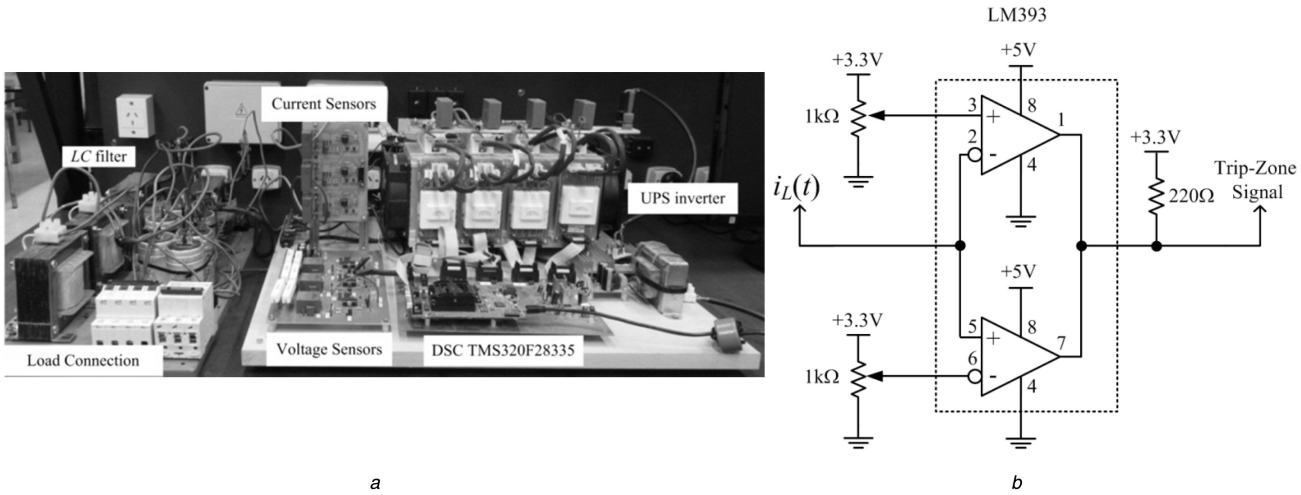

Fig. 4 *Experimental setup and window comparator to obtain a trip-zone signal*
(a) Photograph of the experimental prototype composed by a UPS inverter, DSC, *LC* filter, current and voltage sensors, ***(b)*** Window comparator to obtain a trip-zone signal to limit inductor current during short-circuit faults

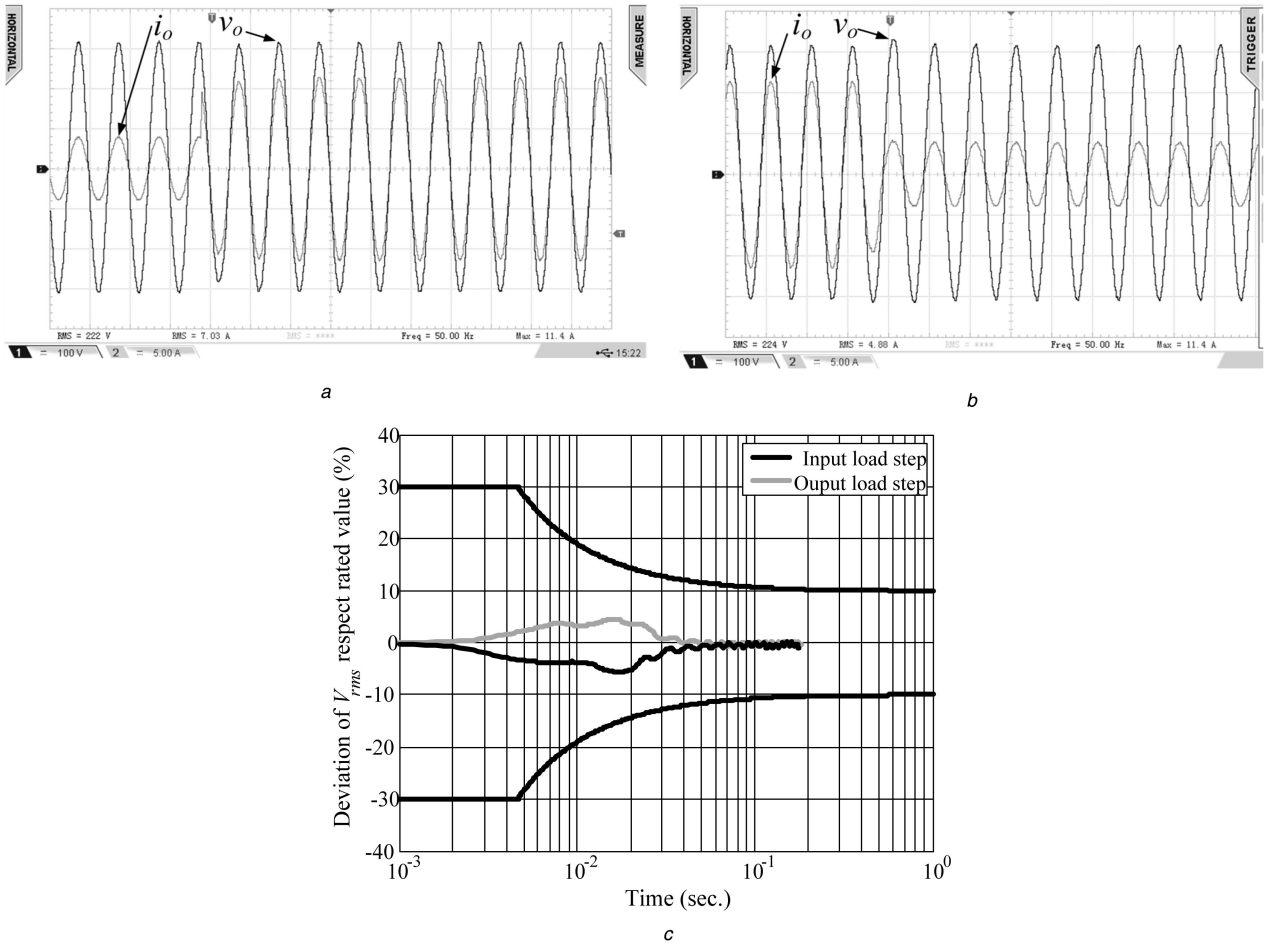

Fig. 5 *Experimental results: transient response of the output voltage and load current*
(a) Step-load variation from 20 to 100% of its rated value. Voltage 100 V/div, current 5 A/div, ***(b)*** Step-load variation from 100 to 20% of its rated value. Voltage 100 V/div, current 5 A/div, ***(c)*** Percentage deviation of the RMS output voltage with respect to its rated value for the step-load variations and limits given in the classification 1 of the Std. IEC 62040-3

what satisfies the requirement of 5% limit of the standard IEEE 519.

Fig. 6*c* shows the output voltage and the inductor current obtained when the inverter operates in steady-state during the no load condition, for the case of using the filter nominal inductance value. When the inductance value is reduced in a 50%, Fig. 6*d* shows the steady-state response of the same variables during no load condition, showing that the inverter operates stably.

As in UPS applications, the filter parameter deviations from their rated values are usually within ±10% of inductance and capacitance [38], and since the inductance variation is more critical than capacitance [16], from the previous results it can be concluded

$$K_{ri\_V} = \left| \frac{(Z_o(z)G_i(z) - G_{ii}(z)G_v(z) - Z_{ov}(z)G_i(z))K_{pi}(G_{ci}(z)+1) + Z_o(z) - Z_{ov}(z) - Z_{ov}(z)G_{ci}(z)K_{pi}K_{pv}G_v(z)}{Z_{ov}(z)G_{ci}(z)K_{pi}G^*_{ri}(z)K_{pv}G_v(z)} \right| \quad (32)$$

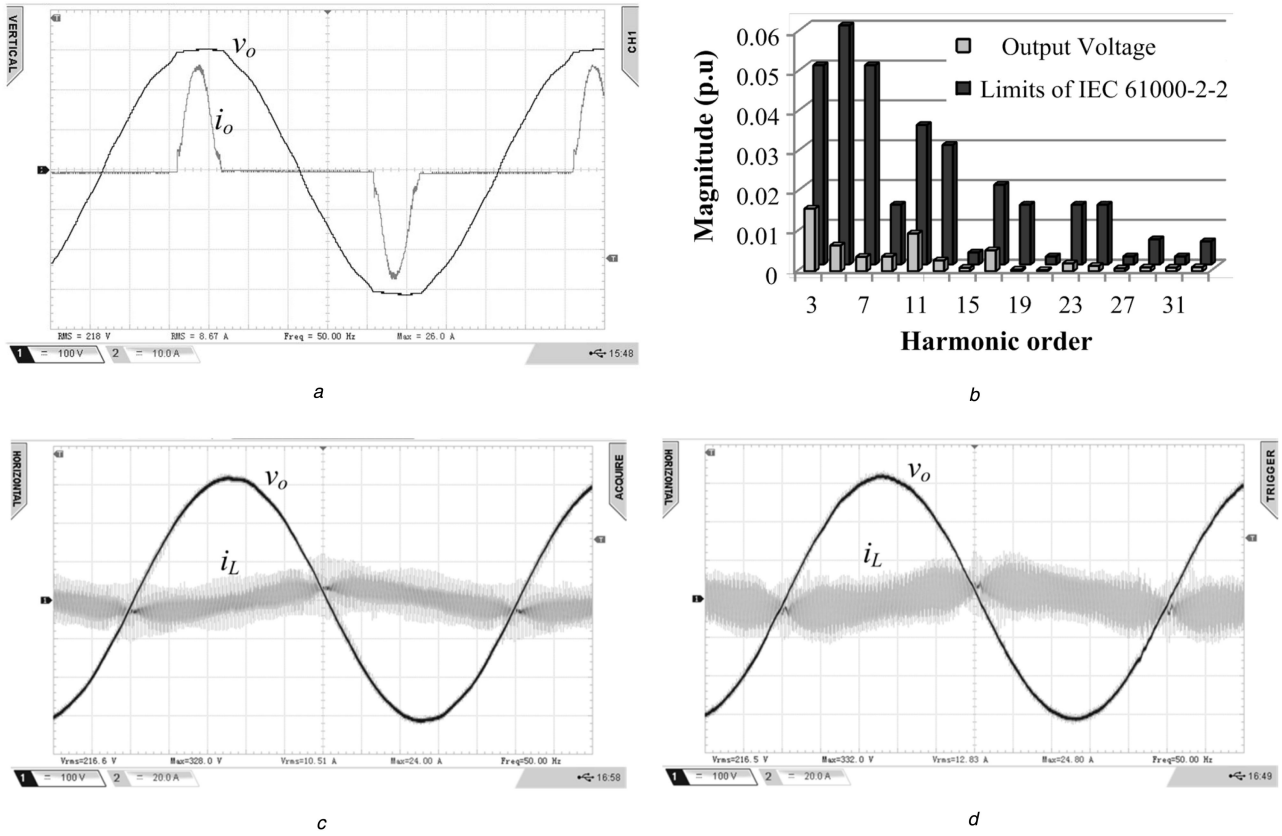

Fig. 6 *Experimental results: steady-state response and harmonic content*

(a) Output voltage and load current in the case of inverter feeding a non-linear load. Voltage scale 100 V/div. Current scale 10 A/div, ***(b)*** Harmonic content of the output voltage in the case of inverter feeding a non-linear load and limits given by the Std. IEC 61000-2-2, ***(c)*** Output voltage an inductor current under no load condition, using the rated *LC* filter inductance (500 μHy), **(*d*)** Output voltage an inductor current under no load condition, using the −50% of rated *LC* filter inductance (250 μHy)

that the system robustness to filter parameter variations is guaranteed by the proposed control strategy and its designed parameters.

Fig. 7*a* shows the transient responses of the output voltage and the inductor current during a short-circuit event. For this experimental result, no window comparator circuit has been used, since the transient current did not trip the driver fault protection circuit. It can be observed that the inner current control loop synthesises a sinusoidal waveform at ∼20 ms after a short circuit occurs, with a steady-state peak value of 22 A, which is a slightly lower than the peak value of 25 A established in the current limiter.

The transient response of the output voltage and the inductor current when a short circuit is cleared are shown in Fig. 7*b*, where it is observed a smooth recovery of the inverter output voltage without overvoltage.

Fig. 7*c* shows the steady-state responses of the output voltage and the output current during an overload event, when a resistive load with an impedance that represents 170% of the rated power is fed, while the overload limit value has been set on 120% of the rated current value. It can be observed that the output current presents a sinusoidal waveform; hence, a sinusoidal output voltage is maintained, as is the objective of the proposed current limiting strategy.

5.2 Experimental results of the PR control strategy

To compare the performance of the plug-in and PR control strategies during the same overload event, Fig. 7*d* shows the steady-state response using the PR structure and its current limiting strategy, where in this case, due to the saturator used on the current reference signal, a distortion in the output voltage can be observed.

Fig. 8*a* shows the transient response during a short-circuit event using the PR structure, where in this case, the window comparator circuit was used to limit the inductor current during the transient. In this experimental result, a similar performance compared to the plug-in control strategy is observed, where a sinusoidal current is synthesised during the third period after the fault occurred.

Fig. 8*b* shows the transient response when the short circuit is cleared, where an overshoot on the output voltage is observed, having a close agreement between the output voltage transient responses obtained with the simulation results of Fig. 3*b*.

5.3 Experimental results of the PR control strategy using only P controller in the inner current control loop

To analyse the performance of the control strategy that uses a PR controller in the outer voltage control loop and P controller in the inner current control loop [17], with the same current limiting strategy proposed in Fig. 1*c*, the resonant controllers in the inner current control loop are eliminated, for which $G_{ci}(z) = 0$. In this case, the phase compensation for $G_{cv}(z)$ can be obtained with the design methodology proposed in [16], while the K_{pv} control action is not required.

Fig. 8*c* shows the transient response during a short-circuit event, where the window comparator circuit was required to limit the transient current. It can be observed that this control strategy presents faster settling times compared to the previous analysed experimental results. The steady-state short-circuit current presents a distortion since there is no tracking capability in the inner current control loop.

Fig. 8*d* shows the transient response when the short circuit is cleared. In this case, it can be observed an output voltage transient recovery without overshoot and with longer settling time than the previous experimental results.

6 Conclusion

In this work, a control strategy to achieve FRT capability and high-performance output voltage was proposed for single-phase UPS inverters. This strategy presents an inner current control loop and an outer voltage control loop, using a plug-in structure based on proportional and multiple resonant controllers, in addition to a

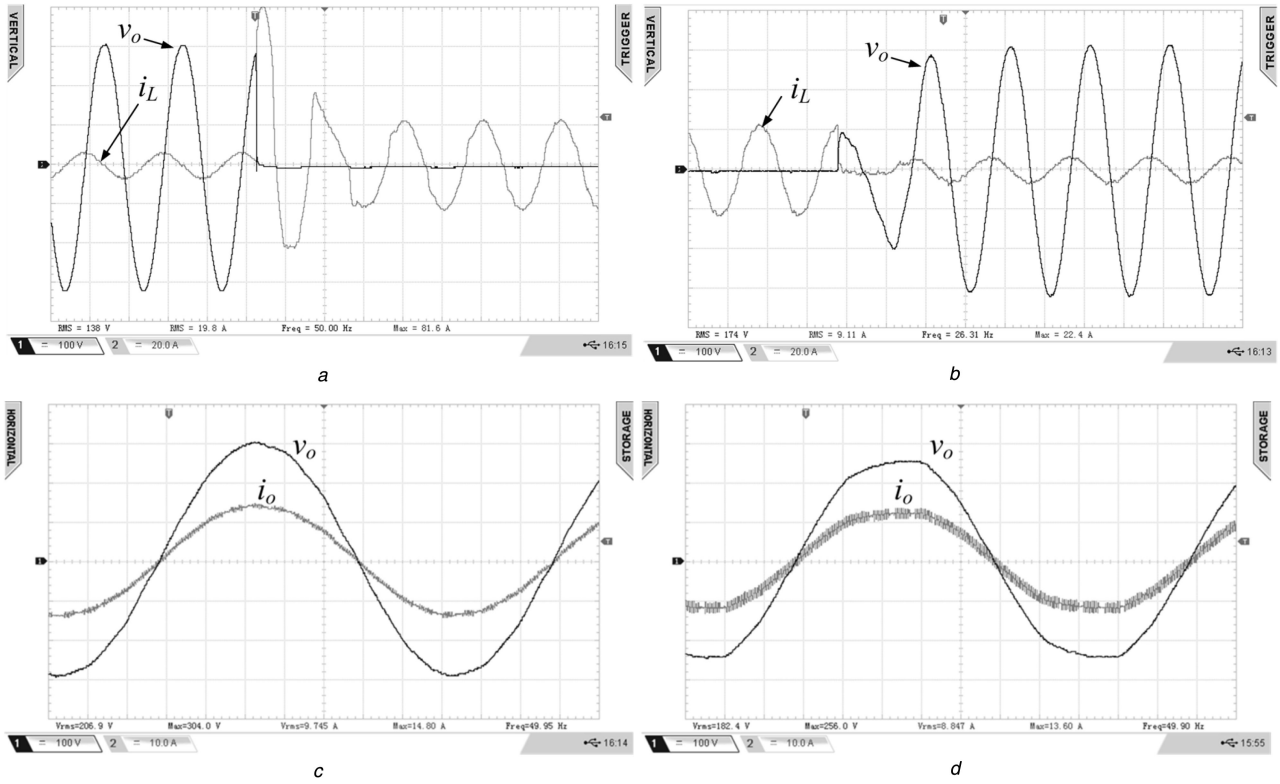

Fig. 7 *Experimental results: transient response during short-circuit and steady-state during overload conditions*

(a) No load to short-circuit condition using plug-in control strategy. Voltage 100 V/div, current 20 A/div, ***(b)***. Short circuit to no load condition using plug-in control strategy. Voltage 100 V/div, current 20 A/div, ***(c)*** Overload using plug-in control strategy. Voltage 100 V/div, current 10 A/div, ***(d)*** Overload using PR control strategy. Voltage 100 V/div, Current 10 A/div

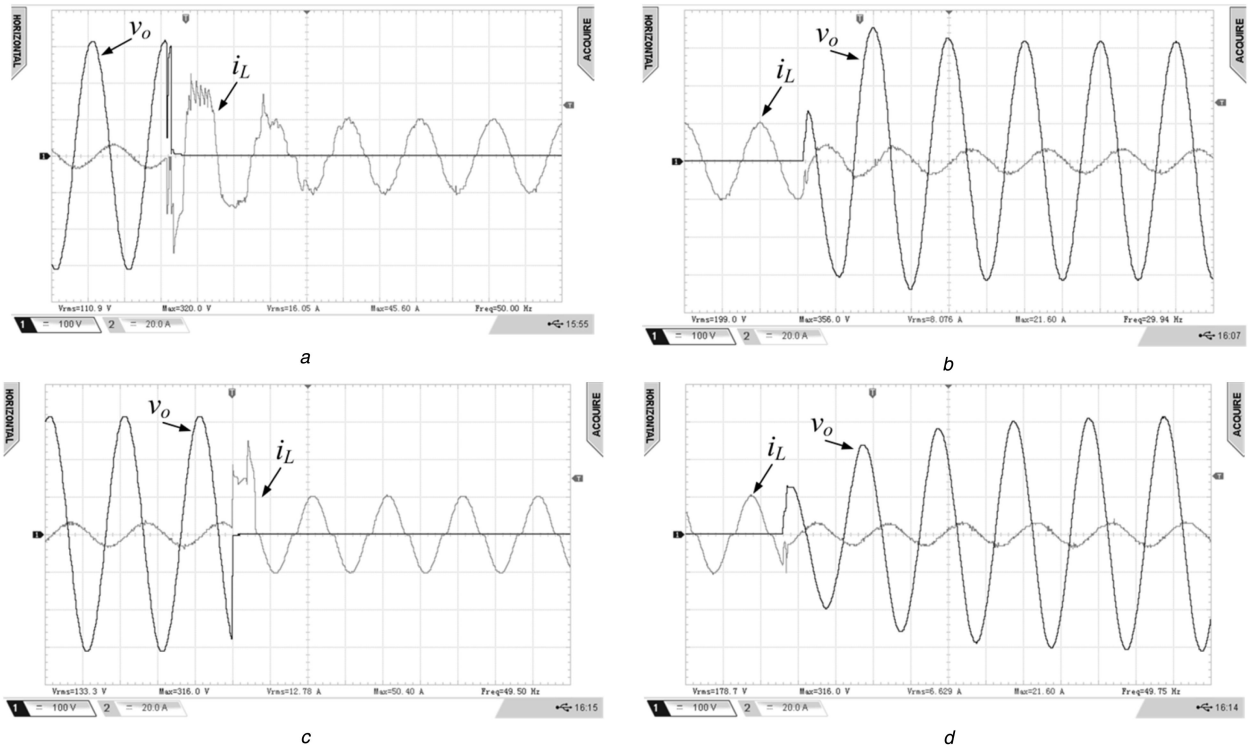

Fig. 8 *Experimental results of transient responses during short circuit*

(a) No load to short-circuit condition using PR control strategy. Voltage 100 V/div, current 20 A/div, ***(b)*** Short circuit to no load condition using PR control strategy. Voltage 100 V/div, current 20 A/div, ***(c)*** No load to short-circuit condition using P control action on the inner current loop. Voltage 100 V/div, current 20 A/div, ***(d)*** Short circuit to no load condition using P control action on the inner current loop. Voltage 100 V/div, current 20 A/div

current limiting strategy to operate during overload and short-circuit conditions.

This particular current limitation allows achieving a distortion-free output voltage in both fault conditions, overload and short circuit, without requiring oversizing the UPS inverter.

By comparing the proposed plug-in control strategy and the conventional PR structure through frequency and time domain analysis, it was shown that the proposed structure improves the output impedance characteristics and the output voltage transient response during FRT events.

With the objectives to achieve wide robustness to parametric uncertainties, a fast dynamic response of the inner current control loop and compliance with UPS power quality requirements, a detailed design methodology of the control loops was proposed.

In order to demonstrate the practical feasibility of the proposal, an experimental 2 kVA inverter prototype was implemented. The results obtained show that the performance of the converter satisfactorily meets the power quality standards for UPS applications, with wide robustness to parametric variation.

FRT performance comparisons between the proposed plug-in control strategy and the conventional PR structure for two cases, (i) PR controller in both control loops and (ii) P controller in the inner current control loop and PR in the outer voltage control loop were obtained. These results show that the proposal presents improved characteristics of the output voltage with respect to the steady-state response during the overload and its recovery after the short circuit, as well as a better transient response of the inductor current in the transition from no load to short circuit.

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